AMENDMENTS TO THE CLAIMS

1. (Currently amended) An image display apparatus comprising:

a display unit for displaying an image, and

a drive unit for driving the display unit, the drive unit being connected by a plurality of signal lines, wherein:

said display unit comprises a plurality of display pixels arranged in a matrix form and the signal lines are arranged in each column, and

said drive unit comprises a ladder resistor, impedance converters each having an input connected to an output of the ladder resistor, gray level voltage wires each connected to the output of the impedance converters, gray level voltage selecting means selectively connecting said gray level voltage wires to said plurality of signal lines, wherein said impedance converters have an offset voltage canceling unit for detecting and eliminating any offset voltage between input and output, and wherein the number of said impedance converters matches the number of said gray level voltage wires and matches a number of a plurality of gray level voltage selectors of said gray level voltage selecting means connected to the gray level voltage wires.

2. (Previously presented) The image display apparatus as set forth in claim 1, wherein said gray level voltage selectors are connected to said plurality of signal lines.

3. (Previously presented) The image display apparatus as set forth in claim 1, wherein said display unit, said gray level voltage selectors and said gray level voltage wires are arranged over the same substrate.

4. (Original) The image display apparatus set forth in claim 1, wherein said impedance converters are configured by drain-grounded field effect transistors.

5. (Original) The image display apparatus as set forth in claim 1, wherein said impedance converters are configured by differential amplifying circuits using field effect transistors.

6. (Canceled)

7. (Original) The image display apparatus as set forth in claim 1, wherein said impedance converters have means for suspending the functioning of the impedance converters and circuits for short-circuiting the input and output terminals of the impedance converters.

8. (Original) The image display apparatus as set forth in claim 1, wherein said display pixels are liquid crystal display pixels each having a counter electrode and a liquid crystal region between the pixel electrode and the counter electrode.

9. (Previously presented) The image display apparatus as set forth in claim 1, wherein said gray level voltage selectors are configured by an analog switch using a field effect transistor, respectively.

10. (Original) The image display apparatus as set forth in claim 1, wherein said ladder resistor is configured by a polycrystalline Si film coped with impurities.

11. (Previously presented) The image display apparatus as set forth in claim 1, wherein said display pixels, said gray level voltage selectors and said impedance converters are configured by polycrystalline Si thin film transistors (TFTs).

12. (Previously presented) The image display apparatus as set forth in claim 1, wherein said display pixels, said gray level voltage selectors and said impedance converters are configured on the same substrate.

13. (Original) The image display apparatus as set forth in claim 1, wherein said ladder resistor is configured by one resistor.

14. (Original) The image display apparatus as set forth in claim 1, wherein said ladder resistor is a pair of resistors, one each for positive voltage gray level generation and inverted voltage gray level generation.

15. (Original) The image display apparatus as set forth in claim 1, wherein said plurality of display pixels are luminescent type display pixels controlled by entered analog image signals and having a light emitting function for displaying an image with luminescence generated by a current flowing between a positive electrode and a negative electrode.

16. (Currently amended) An image display apparatus driving method, comprising:

a step for displaying an image by writing analog image signal voltages via signal lines into pixel capacitances of individual pixels in a display unit, wherein the analog image signal voltages are written into an image display apparatus having a drive unit including a ladder resistor, impedance converters each having an input connected to an output of a ladder resistor, said impedance converters detecting and eliminating any offset voltage, gray level voltage wires each connected to the output of the impedance converters, wherein the number of said impedance converters matches the number of said gray level voltage wires, and matches a number of a plurality of gray level voltage selectors connected to the gray level voltage wires in three separate phases when the analog image signal voltages are written onto the signal lines.

17. (Previously presented) The image display apparatus driving method as set forth in claim 16, wherein the writing of the analog image signal voltages onto said signal lines in said image display apparatus uses impedance converters having offset canceling means using offset canceling capacitances, said method comprising the steps of:

in a first phase, simultaneously with the writing of analog image signal voltages using the impedance converters, writing any offset voltage arising between the input and output voltages of the impedance converters into the offset canceling capacitances;

in a second phase following said first phase, simultaneously with the writing using the impedance converters, canceling any offset voltage of the impedance converters using the offset canceling means; and

in a third phase following said second phase, writing analog image signal voltages directly onto the signal lines without going through the impedance converters.

18. (Original) The image display apparatus driving method as set forth in claim 16, wherein said signal lines are provided with voltage resetting circuits, and analog image signal voltages are written in three separate phases after the voltages of the signal lines are reset in advance by the resetting circuits.

19. (Currently amended) A driving method comprising:

a step for displaying in an image display apparatus having a plurality of display pixels arranged in a matrix form to display an image, a group of signal lines provided for each column to transmit analog image signals and connected to the display pixels, and a drive circuit for driving the display pixels and the group of signal lines at prescribed timings, and writing the analog image signal voltages into the pixel capacitances of the display pixels to display an image, wherein:

said drive circuit having a ladder resistor and a plurality of gray level voltage wires each connected through a plurality of impedance converters, respectively to an output of the ladder resistor, said impedance converters detecting and eliminating any offset voltage;

said group of signal lines are connected to said gray level voltage wires via a gray level voltage selector;

each gray level voltage wire is connected to the output of the impedance converters, respectively, wherein the number of said impedance converters matches the number of said gray level voltage wires;

at least the display pixels, the group of signal lines, the gray level voltage selector and the gray level voltage wires are provided over the same substrate; and

wherein the analog image signal voltages are written in three separate phases when the analog image signal voltages are to be written onto the signal lines.

20. (Currently amended) An image display terminal system, comprising:

a plurality of display pixels arranged in a matrix form to display an image;

a group of signal lines provided for each column to transmit analog image signals and connected to the display pixels;

a drive circuit for driving the display pixels and the group of signal lines at prescribed timings; and

means for causing the display pixels to display an image in a prescribed sequence on the basis of inputted image display data, wherein:

said drive circuit has a ladder resistor and a plurality of gray level voltage wires each connected through a plurality of impedance converters, respectively to an output of the ladder resistor;

said group of signal lines are connected to the gray level voltage wires via a gray level voltage selector;

each of said gray level voltage wires connected to the output of the impedance converters, respectively, wherein the number of said impedance converters matches the number of said gray level voltage wires, wherein said impedance converters have an offset voltage canceling unit for detecting and eliminating any offset voltage between input and output; and

at least the display pixels, the group of signal lines, the gray level voltage selector and the gray level voltage wires are provided over a single substrate.

21. (Previously presented) The image display terminal system as set forth in claim 20, wherein said impedance converters are buffer amplifiers.

22. (Previously presented) The image display apparatus as set forth in claim 1, wherein said impedance converters are buffer amplifiers.